MARIA TECHNOLOGY™, by General Computer Corp., makes available a hardware and software breakthough in low-cost high-speed color text and graphics display for personal and business systems.

FEATURES

- Prioritized display-list data structure, providing greater screen image complexity than conventional "sprites" and faster interactive response than multi-plane "bit map" screen buffers.
- DMA processor and local registers to periodically halt the host processor and access zone pointers, display-list pointers, object position and width parameters, and then process graphics data.
- Real-time scan-line image composition LINERAM with 320-pixel resolution, automatic last-object prioritization, automatic transparency, and previous-scanline video output buffer.
- Dynamic writeable COLOR MAP with 8 palettes of 3 colors, plus background color available as 4th color in each palette. Video output of color values defined as 4 bits luminance plus 4 bits chrominance (with on-chip color phase shifter).
- Interface compatibility with conventional microprocessor bus systems, NTSC and PAL television standards and popular television interface adapter schema, e.g. Atari 2600.

Part Type:	GCC 1702	GCC 1712	GCC 1722
Bus System:	6502/6800	6502/6800	680X0
Video Type:	NTSC	PAL	NTSC + PAL
Package Type:	48 PDIP	48 PDIP	68 PLCC
Temp Range:	0 - 70 °C	0 - 70 °C	0 - 70 °C
Status 10/84:	Available	Prototype	Definition

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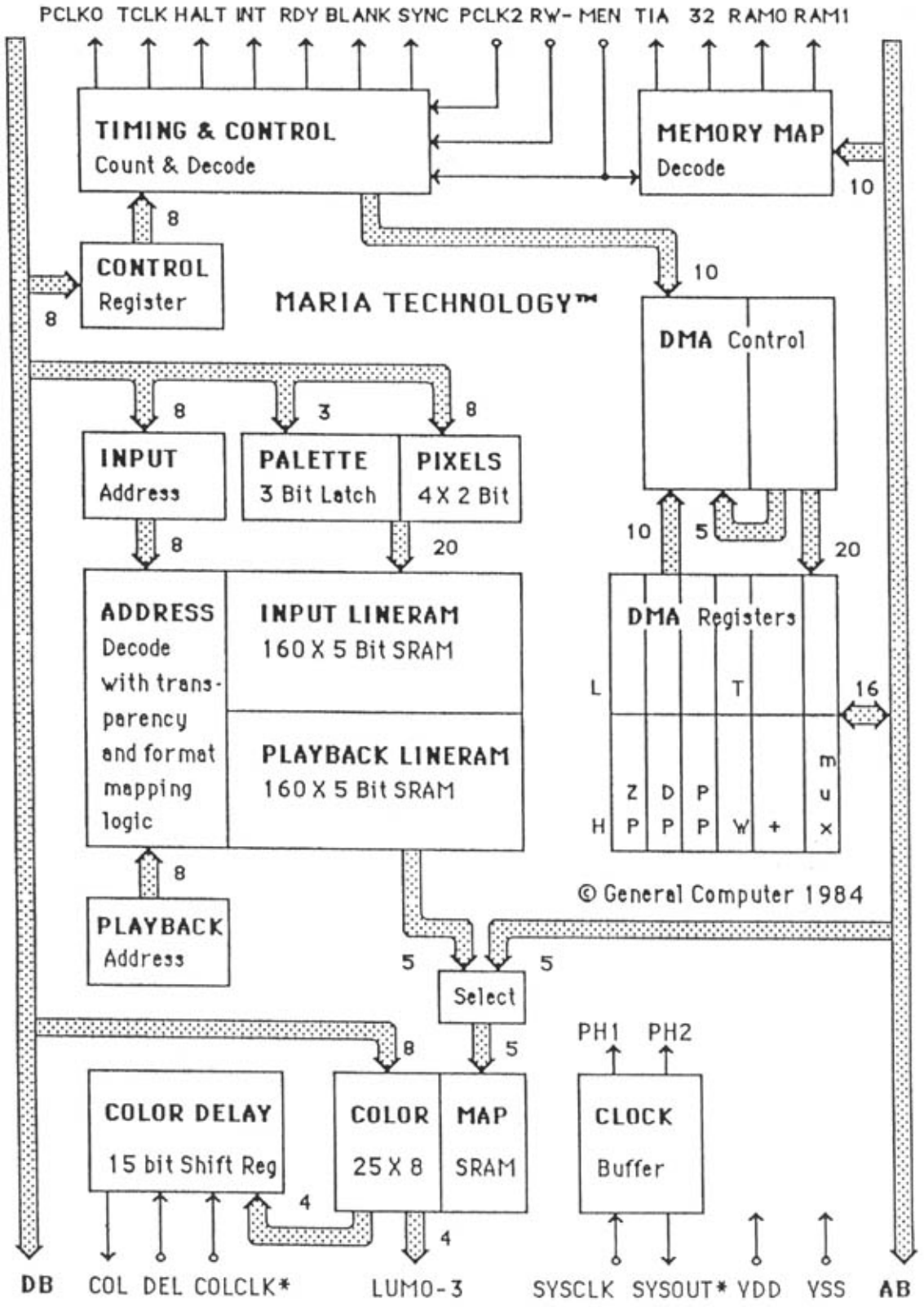
Figure 1. Block Diagram



1.0 Pin Descriptions

The following table gives a description and polarity (NAME- indicates asserted low) for each pin:

NAME	PIN	TYPE	DESCRIPTION
VSS	1	P	Ground.
INT-	2	O	Interrupt request output. Drive capability: one MOS load.
COLCLK*	3	I	Color subcarrier reference clock: 4.433618 Mhz ± 250Hz. (* means PAL only: part type GCC 1712 or 1722).
SYSOUT*	3	O	Self-oscillator output for series-resonant 14.31808 MHz crystal. (* means part type GCC 1702 only).
SYSCLK	4	I	System Clock input 14.31808 Mhz ± 1%. External timing is a submultiple of this system clock.
MEN	5	I	Maria ENable input. When high, allows full Maria operation. When low, video is shut off, chip is held in reset, and memory map is set for 2600-mode. On-chip 3-6K pulldown resistor.
PCLK2	6	I	Ø2 processor clock output, used to handshake with processor. (However,some handshaking uses open-loop control based on synchronuous timing of Maria's internal PCK0).
TCLK	7	O	TIA 3.58 MHz clock. SYSCLK frequency divided by 4. Drive capability: one MOS load.
PCLK0	8	O	Ø0 processor clock input. Runs at SYSCLK divided by 8 or 12, depending on memory map. Drive capability: one MOS load.
DEL	9	I	Control voltage (unbuffered low-resistance analog input) for adjusting video output COLOR DELAY shift register.
RAM0-	10	O	RAM0 chip select output. Drive capability: one MOS load.
AB0 thru AB11	11 thru 22	I/O	Address input (when microprocessor is in control) or output (during DMA). Drive capability: 150 pF + 2 LS loads.
32-	23	O	6532 chip select output. Drive capability: one MOS load.
RAM1-	24	O	RAM1 chip select output. Drive capability: one MOS load.
VDD	25	P	5.00V ± 0.25V power supply.
TIA-	26	O	TIA chip select output. Drive capability: one MOS load.

1.0 Pin Descriptions (continued)

NAME	PIN	TYPE	FUNCTION
AB12 thru AB15	27 thru 30	I/O	Address input (when microprocessor is in control) or output (during DMA). Drive capability: 150 pF + 2 LS loads.
DB7 thru DB0	31 thru 38	I/O	Data input or output. Drive capability: 150 pF + 2 LS loads.
R/W-	39	I	Microprocessor R/W- output. 3-6K on-chip pullup resistor.
HALT-	40	O	Bus request output. Drive capability: one MOS load.
RDY	41	O	"Ready" output. Open-drain with on-chip 3-6K pullup resistor. Drive capability: one MOS load.
LUM0	42	O (TS)	Least-significant video luminance output bit. Pad tri-states when MEN is not asserted. Drive capability: 2 LS loads.
CCL	43	O (TS)	Color output. Pad tri-states when MEN is not asserted. Drive capability: 2 LS loads.
LUM3	44	O	Video luminance outut pin. Pad goes low when MEN is not asserted. Drive capability: 2 LS loads.
LUM2	45	O	Video luminance outut pin. Pad goes low when MEN is not asserted. Drive capability: 2 LS loads.
BLANK	46	O	Video composite-blanking output pin. Pad tri-states when MEN is not asserted. Drive capability: 2 LS loads.
LUM1	47	O	Video luminance outut pin. Pad goes low when MEN is not asserted. Drive capability: 2 LS loads.
SYNC	48	O	Video composite-sync output pin. Pad goes low when MEN is not asserted. Drive capability: 2 LS loads.
DB15 thru DB8	NA	I/O	GCC 1722 only. Data input or output. Drive capability: 150 pF + 2 LS loads.

Notes on TYPE:	
I	input
O	output
I/O	bidirectional (implies tri-state output when used as input)
(TS)	tri-statable
P	power

2.0 Description of Functions

The primary objective of MARIA TECHNOLOGY™ is to provide low-cost high-speed graphics. Five major functions support this objective: microprocessor interface, display-list DMA, LINERAM processing, dynamic COLOR MAPing, and video output. With reference to the labels on the block diagram (Figure 1), following is a description of each major function:

2.1 Microprocessor Interface

TIMING & CONTROL count and decode logic synchronizes the Maria chip to video timing, providing SYNC and BLANK signals. Synchronous with this video timing, a 1.79MHz processor clock PCLK0 and a 3.58MHz TCLK are produced; and the HALT- signal is produced to periodically request bus control. The busses are available for display-list DMA operation after the bus cycle when HALT- is asserted. Microprocessor operation resumes the next bus cycle after HALT- is de-asserted.

MEMORY MAP decode logic produces chip selects for 4 external chips, plus an internal (Maria) select. The external selects are TIA-, 32-, RAM0- and RAM1-. There is also logic to slow the clock when an address falls on the TIA or 6532 space, stretching the normal1.79 Mhz PCLK0 equivalent to an operating speed of 1.19 Mhz. The system memory map implemented for the initial Maria chips (GCC 1702 and 1712) is shown in Figure 2 on page 9.

The one-byte CONTROL register (address 3C) is written to by the processor to set various modes. The format is: CONTROL [7 thru 0] = [CK DM1 DM0 CWIDTH BCNTL TK RM1 RM0]

BIT	MEANING
CK	Color Kill. CK = 1 sets COL to logic 1, eliminating color artifacts for text modes.
DM1 DM0	0 X Test Mode (Not for program use: Does not assert HALT-) 1 0 Run normally. 1 1 Inactive.
CWIDTH	Character map WIDTH. CWIDTH = 1 causes 2 bytes of graphics to be fetched for each map byte, CWIDTH = 0 causes 1 byte of graphics to be fetched for each map byte.
BCNTL	Border CoNTroL. BCNTL = 1 causes the background color, P0C0, to extend into horizontal overscan. BCNTL = 0 forces overscan to be black.
TK	Transparency Kill. TK = 1 disables transparency. Useful for some 320 modes.
RM1 RM0	Lineram Read Mode (see graphics mode table)

Over-riding the various modes set by writing to the CONTROL register, one mode (2600-mode) is selected by de-assertion of the MEN (Maria ENable) pin. In this mode, the function of the Maria chip is to provide chip select signals address mapping identical to that of the Atari 2600 VCS unit. The Maria chip is otherwise held in a passive reset state, with it's bus and video outputs turned off.

In addition to the CONTROL register, there are other Maria registers which are written to or read by the microprocessor, including WaitSYNC and STATusReaD which are used to synchronize program to video timing, and 25 COLOR MAP registers. The full register map is shown in Figure 3 on page 10.

2.2 Display-list DMA

The description of the television picture is raster-oriented. The picture is composed in real time (except for one scanline of buffering) on a scanline-by-scanline basis. Contiguous scanlines (usually 8 or 16) are grouped into zones which have a common pictoral structure, or display-list.

The current item (object) in a display-list is pointed to by the DISPLAY-LIST POINTER (Maria register pair DPH/L). DMA operation is used to read the display-list once for each scanline in the zone. The display list has been previously created by the microprocessor program -- in response to user inputs. The DMA processor halts the microprocessor to read display-list items.

Each item in the display-list describes an object, and contains the WIDTH in bytes, position (initial INPUT address), PALETTE, and base address PIXEL-POINTER of the graphics data (Maria register pair PPH/L). An OFFSET is added to that base address. OFFSET is set to one less than the zone size at the beginning of each zone, and decremented at the start of each new scanline.

Using OFFSET and display-lists means minimal RAM space for image composition: The top-level structure of the picture remains the same over several scanlines -- while the detailed graphics is different on each scanline. After reading an object description, the graphics bytes (4 PIXELS each) pointed to are read, decrementing WIDTH and incrementing INPUT position until WIDTH is zero.

For text there is an alternative to fetching graphics directly. Some items in a display-list may use a character map which points to character graphics (usually in ROM), by setting their indirect (IND) bits. In this case the CHARBASE register (previously set up by the microprocessor) is concatenated with the character map byte and OFFSET is added, to form the pointer to the character graphics.

To compose a full screen image, display-lists are grouped into a list of zones. The current zone in the zone-list is pointed to by the ZONE-POINTER, which is also a Maria register pair (ZPH/L). Each zone-list item contains the DP, initial OFFSET and "holy DMA" and DLIen mode bit information for the zone. The zone-list items are read sequentially, one for each zone. The next zone-list item will be read immediately after completion of the last display-list in the current zone (i.e. after OFFSET decrements to zero). The sum of zonesizes (initial OFFSETs) of the zone-list items must add to the number of active scanlines (242 for NTSC or 292 for PAL).

Setting the"holy DMA" bits A12ENable or A11ENable enables checking for "invalid" graphic addresses: Detection of PP + OFFSET addresses with A12 or A11 = 1 results in aborting the object that requested the address. This feature is used to save the DMA time that would be used by objects that are "invisible" in a zone, without actually deleting those objects from the list. It also saves ROM space: No "blank" graphics data is necessary.

Setting the DLIen bit causes the Maria chip to generate an INT- to the microprocessor at the completion of the zone DMA. This allows real-time re-programming.

There is no fixed limit on the number or size of the objects that can be displayed. There is a time limit (somewhat less than one scanline - 64 us) before DMA is automatically terminated, however. Thus the upper bound on screen complexity is set by the amount of DMA time available. The only restriction is that the size and number of objects be such that they can be completed in the time available). The formats for display-lists and zone-lists is shown in Figure 4 on page 11.

2.3 LINERAM Processing

The result of DMA for each item in each display-list in each zone-list is to fetch the WIDTH and initial horizontal INPUT address, a single PALETTE and a variable number of PIXELS for the next object. An object occupies a rectangle: an integral multiple of pixels across and zones in height.

In the primary "160A" graphics mode, each byte of graphics is divided into four 2-bit PIXEL color codes, which are each combined with the PALETTE code. Thus four 5-bit color codes (PALETTE + PIXEL) are simultaneously written to the INPUT LINERAM for each byte, beginning at the initial INPUT address, which is permitted to fall on any pixel boundary. Every three 140-nsec cycles another graphics byte is fetched, and another 20 bits of color codes are written to the INPUT LINERAM, incrementing INPUT and decrementing WIDTH -- until WIDTH is zero.

If WIDTH specifies that 31 bytes be so written for a large object, that single item in a display-list in a zone-list will result in 124 X 5 bits of color codes being written -- in approximately 13 microseconds. This illustrates the bandwidth compression effect which MARIA TECHNOLOGY™ provides: 124/160 of a scanline being written in 13/64 of the available time means there is some time left over, e.g. for running the program to achieve quick interactive response to user inputs.

Another use of bandwidth-compression time is prioritization, i.e. which object is on top. The program controls the overlapping of objects by ordering the display-list items to be written to the INPUT LINERAM. The last object written will end up "on top" of anything written before it.

An automatic transparency feature is also available, when the TK bit in the CONTROL register is zero, to handle partially overlapping objects. When an object that does not fill its rectangle, e.g. a circle, overlaps another object, part of the underlying object should show. For this purpose, the '00' color in each palette is reserved as "transparent". The INPUT LINERAM has logic that detects '00' PIXEL bits and suppresses writing of such PALETTE + PIXEL color codes.

In addition to the 160A graphics mode, other pixel/palette formats are provided. For text, the "320A" format effectively divides each 160A 2-bit pixel code into two sequential1-bit pixel codes. So while 160A provides 2-bit pixel codes in each of 8 palettes, 320A has only 1-bit pixel code in each of 8 palettes -- but has the capability to do 320-across text (40 8-pixel character maps).

Numerous screen effects are supported using different palette/pixel COLOR graphics formats which are set by the WriteMode bit fetched in five-byte display-list items and the ReadMode1 ReadMode0 bits written to the CONTROL register. The graphics formats are shown in Figure 5 on page 12.

At the end of each scanline the INPUT LINERAM and the PLAYBACK LINERAM swap roles, and the scanline that was just composed is sequentially read via the COLOR MAP and video output to the TV.

2.4 Dynamic COLOR MAP

A 5-bit COLOR code for each pixel output from the PLAYBACK LINERAM is used to select one of the 8-bit COLOR MAP registers, which were previously written to by the microprocesssor to define their luminance and chrominance values. This provides data compression, avoiding the extra LINERAM capacity and (more importantly) avoiding the extra DMA time which would otherwise be needed to store an eight-bit color definition for each LINERAM pixel.

2.4 Dynamic COLOR MAP (continued)

The 5-bit COLOR code is interpreted as 3-bit PALETTE + 2-bit PIXEL code, except that all palettes share a common 'background' register for the '00' pixel code. This is done because it is desirable for all objects in the system to share a common "background" color that they are displayed against. Hence, there are three unique color registers in each of eight palettes, plus the shared 'background' color register, for a total of 25.

The COLOR MAP output is composed of four bits of luminance and four bits of chrominance data. The least significant four bits are luminance outputs, while the most-significant four bits are inputs to the color phase-shift circuit. The pipelined COLOR MAPing circuitry runs at 7 MHz, which is the rate required to support 320-pixel scanline resolution.

Images with more than 25 colors (up to 226 distinct chrominance/luminance values) are supported by dynamically re-writing to COLOR MAP registers. It is preferable for the processor to write to COLOR MAP registers during BLANK. However, if the processor writes to a COLOR MAP register during on-screen mapping, the previous output of the COLOR MAP is held over until the processor is done -- in effect stretching an existing pixel color on the screen horizontally for that one cycle, rather than have a wholly unexpected color (the one being written in) appear on the screen as a glitch. In regions of solid color (e.g. the screen border) the effect is invisible.

2.5 Video Output

Video output circuitry produces a close approximation to NTSC and/or PAL television standards. The LUM, COL, BLANK and SYNC signals can be summed through an external resistor network to form a composite video signal.

The COLor circuitry uses an analog input voltage (the DEL pin) to adjust an internal multi-tap shift register delay line. The chroma sub-carrier for NTSC is a 3.58MHz clock divided down from the 14.32MHz SYSCLK and controllably phase-delayed to any of 15 angles (0 to 336°) with respect to the colorburst signal which is output after each horizontal SYNC pulse. The chroma sub-carrier for PAL is an external 4.43 MHz COLCLK, with the color bursts generated at ± 132 degrees (internal delay-line taps 2 and 13) with 180 deg. (yellow) at tap no. 15.

SYNC counters define the screen layout as 454 cycles of the internal 7MHz clock per scanline, with 263 or 313 scanlines per field (for NTSC or PAL, respectively). The screen is not interlaced. NTSC and PAL screen layouts indicating the horizontal and vertical counts delineating border, BLANK and SYNC are shown in Figure 6 on page 13.

3.0 Parametric Specifications

Input/output DC specifications and absolute maximum ratings are shown in Figure 7 on page 14.

Timing specifications are shown in Figure 8 and 9, on pages 15 and 16 respectively.

Figure 2. Memory Map

AB15	14	13	12	11	10	9	8	7	6	5	pav	HALT-	MEN = 1 OUTPUT	
0	0	0	0	0	1	0		1					6532-	480- 4FF
														580- 5FF
0	0	0	0	0	0	1		1					6532-	280- 2FF
														380- 3FF
0	0	0	1	1								1	RAM1-	1800-1FFF
0	0	0	1	1							1	0	RAM1-	1800-1FFF
0	0	0	0	0	0			0	0	0			TIA-	0- 1F,
														100- 11F,
														200- 21F,
														300- 31F
0	0	0	0	0	0			0	0	1	*		par23	20- 3F
0	0	0	0	0	0			1				1	RAM0-	80- FF
0	0	0	0	0	0			1			1	0	RAM0-	80- FF
0	0	0	0	0	0			0	1			1	RAM0-	40- 7F
0	0	0	0	0	0			0	1		1	0	RAM0-	40- FF,
														140- 1FF,
														240- 2FF,
														340- 3FF
0	0	1	0	0								1	RAM0-	2000-27FF
0	0	1	0	0							1	0	RAM0-	2000-27FF
0	0	0	0	0	0			0	0	0			slow (TIA)	
0	0	0	0	0	1	0		1					slow (6532)	
0	0	0	0	0	0	1		1					slow (6532)	

2600 mode:

AB15	14	13	12	11	10	9	8	7	6	5	pav	HALT-	MEN = 0 OUTPUT	
			0					1					6532-	80- FF
			0					0					TIA-	0- 7F
													slow	

Notes: Blank entries indicate don't-care conditions.

"par23" is the internal Maria select.

"pav" is "Processor Address Valid," an internal signal which is internal version of PCLK0 OR'ed with internal PCLK2.

"*" indicates "par23" does not have "pav" in its equation when HALT- is asserted.

"slow" indicates a device which runs at a clock of 1.19 MHz, rather than 1.79 Mhz.

Figure 3. Register Map

Address	Register	Comments	
20	P0C0	**Background Color**	(COLOR MAP registers 0,4,8,12,16,20,24,28)
21	P0C1	**Palette 0, Color 1**	(COLOR MAP registers are write-only)
22	P0C2	**Palette 0, Color 2**	
23	P0C3	**Palette 0, Color 3**	
24	WSYNC	**Wait for SYNC**	(Writing to this location de-asserts RDY, which is asserted again at the completion of the current scanline -- synchronizing program to video timing.)
25	P1C1		
26	P1C2		
27	P1C3		
28	STATRD	**STATus ReaD [7 thru 0] = [VBlank 0 0 0 0 0 0 0]** (Read only)	
29	P2C1		
2A	P2C2		
2B	P2C3		
2C	ZPH	**Zone Pointer, high byte.**	
2D	P3C1		
2E	P3C2		
2F	P3C3		
30	ZPL	**Zone Pointer, low byte.**	
31	P4C1		
32	P4C2		
33	P4C3		
34	CHARBASE	**The upper byte of character-map addresses.** (Lower byte is in the map, i.e. the character code.)	
35	P5C1		
36	P5C2		
37	P5C3		
38	unused	**Write in 0**	(Reserved for future enhancements)
39	P6C1		
3A	P6C2		
3B	P6C3		
3C	CONTROL	**[7 thru 0] = [CK DM1 DM0 CWIDTH BCNTL KM RM1 RM0]**	
3D	P7C1		
3E	P7C2		
3F	P7C3		

Figure 4. List Formats

The microprocessor program sets up for zone-lists and display-lists with the following formats:

Zone-list format:

```
< DLIen A12en A11en  0  OFFSET[3 thru 0] >
<DPL>
<DPH>
  .
  .                    (Items for enough zones to cover all active scanlines)
  .
```

Note: OFFSET value is (n-1) scanlines, e.g. use OFFSET = 7 for 8 lines.

Display-list formats:

```
<PPL >
<  PALETTE[2 thru 0] WIDTH[4 thru 0] >          (Non-zero WIDTH)
<PPH >
<INPUT>
  .
  .                    (Four and five-byte formats may be used in any order)
  .
<PPL>
<  WM 1 IND 0 0 0 0 0 >
<PPH>
<  PALETTE[2 thru 0] WIDTH[4 thru 0]  >
<INPUT>
  .
  .                    (Items repeat until a Null Item format is encountered)
  .
<PPL>
<  0  >                (Null Item format:  ends display-list DMA operation)
```

Notes: WM is new value of lineram write-mode bit for this and succeeding objects (until changed by another long header). IND is indirect mode for this object ONLY. WIDTH is a two's complement representation of width; 11111 is a one-byte wide object or character map. WIDTH field is not checked for all zeroes on LONG headers. Display lists, zone lists and character maps must be in fast (RAM) memory.

DMA Cycles (approximately 140ns each):

Four-byte format	8	
Five-byte format	10	
Graphics, per byte	3	
Character map fetch	3	(plus one or two graphics fetches, depending on CWIDTH)
DMA Startup	5-12	
DMA Shutdown, short	13-17	(after the last line in a zone, when the next item is fetched)
DMA Shutdown, long	19-23	(after the last line in a zone, when the next item is fetched)
End-Of-VBlank DMA	7	(used to fetch the first zone-list item in the next screen)

Figure 5. Graphics Formats

MODE	[WM	RM1	RM0]	COLOR	[4	3	2	1	0]
160A	0	0	X		P2	P1	P0	G7	G6
								G5	G4
								G3	G2
								G1	G0
160B	1	0	X		P2	G3	G2	G7	G6
						G1	G0	G5	G4
320A	0	1	1		P2	P1	P0	G7	0
								G6	0
								G5	0
								G4	0
								G3	0
								G2	0
								G1	0
								G0	0
320B	1	1	0		P2	0	0	G7	G3
								G6	G2
								G5	G1
								G4	G0
320C	1	1	1		P2	G3	G2	G7	0
								G6	0
						G1	G0	G5	0
								G4	0
320D	0	1	0		P2	0	0	G7	P1
								G6	P0
								G5	P1
								G4	P0
								G3	P1
								G2	P0
								G1	P1
								G0	P0

Notes: WM is part of the display list and affects the current INPUT LINERAM. RM0 and RM1 are CONTROL register bits and affect the current PLAYBACK LINERAM.

Pn represents palette bits. Gn represents graphics data bits. The topmost PIXEL data in the table comes out first (i.e. is displayed left-most on the screen).

Blank COLOR bit entries indicate same value as above in each column; e.g., all 160A COLORs have palette bits as the three most-significant COLOR bits.

Figure 6. NTSC & PAL Screen Layouts

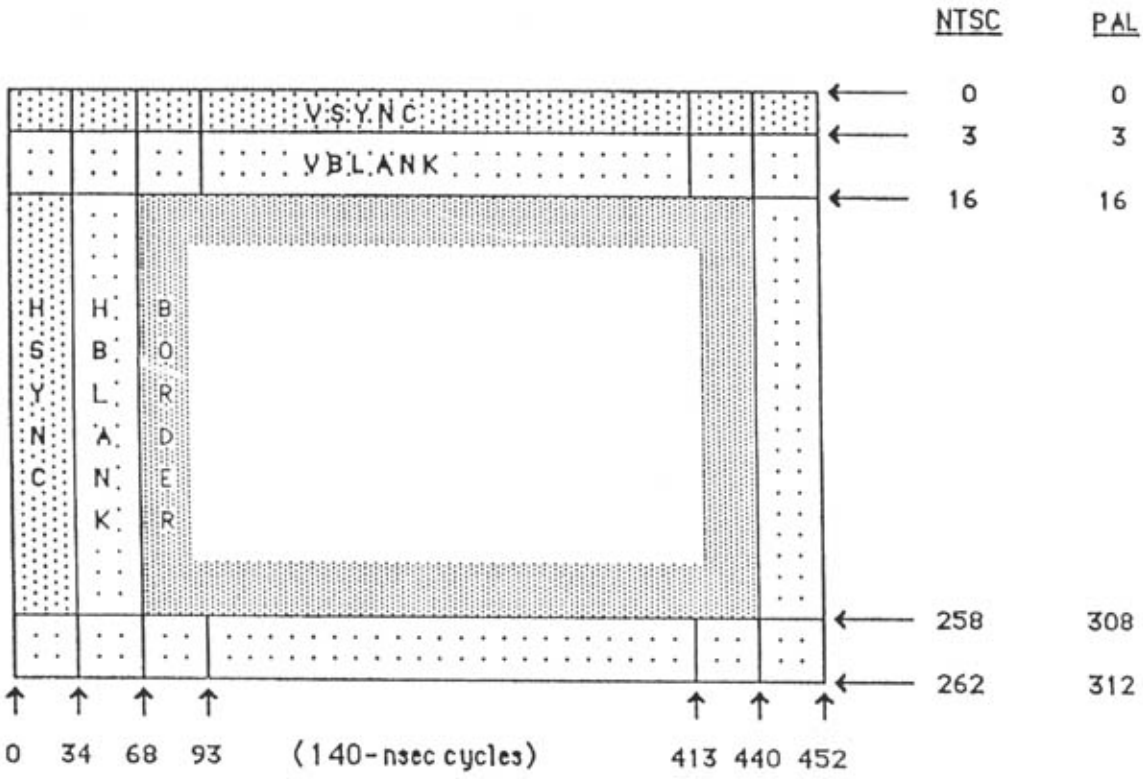


Figure 7. D.C. Specifications

Input/Output Levels (Ta = 0 to 70 deg C, Vdd = 4.75V to 5.25V)

Parameter (Level)	Sym	Min	Max	Units	Conditions
Input Voltage - Low	Vil	---	0.8	Volts	
Input Voltage - High	Vih	2.0	---	Volts	
Output Voltage - Low	Vol	---	0.4	Volts	Iol = +2.0 ma
Output Voltage - High	Voh	2.4	---	Volts	Ioh = -400 ua
Output Current - Low	Iol	---	+2.0	mA	Vol = 0.4 V
Output Current - High	Ioh	---	-400	uA	Voh = 2.4 V
Output Leakage - TS	Its	---	±20	uA	Vin = 0 to Vdd
Power Supply Curr	Idd	---	185	mA	
Input Leakage	Ili	---	±10	uA	Vin = 0 to Vdd
Delay Adjust Voltage	Vdel	0.0	6.0	Volts	

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Operating Voltage (VDD)	4.75	5.25	Volts
Storage Voltage (any pin, referenced to VSS)	-0.5	+7.0	Volts
Static Test (any pin, 883 circuit)		500	Volts
Operating Temperature (Ambient)	0	70	°C
Storage Temperature (Ambient)	-25	+125	°C

Figure 8. Timing Specifications

(Ta = 0 to 70 deg C, Vdd = 4.75V to 5.25V)

High-speed DMA (Zone-list, display-list, and character map accesses):

Time (nsec)	Symbol	Min	Max
ABn, output valid after ph2 goes high	T(dlABpd)		80
Chip selects, output valid after ph2 goes high,RAM0CS-, RAM1CS-	T(dlCSpd)	100	
DBn, input valid before ph2 goes high	T(dlDBsu)	15	
DBn, hold time after ph2 goes high	T(dlDBh)	0	
RAM access time = 4*SYSCLK period - (T(dlDBsu) + T(dlCSpd))	T(dlRacc)		165

Low-speed DMA (Graphics accesses):

Time (nsec)	Symbol	Min	Max
ABn, output valid after ph2 goes high	T(gABpd)		100
DBn, input valid before ph2 goes high	T(gDBsu)	15	
DBn, hold time after ph2 goes high	T(gDBh)	0	
Chip selects, output valid after ph2 goes high: RAM0-, RAM1-	T(gCSpd)		120
ROM access time = 6*SYSCLK period - (T(gDBh) + T(gCSpd))	T(gRacc)		285

Microprocessor

Time (nsec)	Symbol	Min	Max
ABn and R/W-, inputs valid before PCLK0 goes high (1.79MHz cycle)	T(upABsu)	60	
Chip selects valid after PCLK0 goes high: TIA-, 32-, RAM0-, RAM1-	T(upCSpd)		40
DBn, input valid before PCLK0 falls	T(upDBsu)	40	
DBn, input hold time after PCLK0 falls	T(upDBh)	0	
DBn, output valid before valid before PCLK0 (held through PCLK2.)	T(upDBpd)	70	
ABn, input valid before PCLK0 goes high with (1.19 Mhz cycle)	T(upABsu)	60	

Notes:

Timings are specified for pin loading conditions listed in section 1.0 on pages 2 and 3, with MOS load = 20pF and LSTTL load = +100 to -400uA current source + 20pF. Current into a device or load is positive.

Because PH2 is an internal Maria signal, external system timing during DMA is referenced to SYSCLK. PH2 is generated by dividing SYSCLK by 2, and the toggle flip-flop may initially come up in either the logic 0 or 1 state. The active edge of SYSCLK for the divide-by-2 logic is the negative transition. By observing the relationship of PCLK0 (which is synchronized by PH2) to SYSCLK, the relationship of PH2 to SYSCLK may be inferred.

Figure 9. Timing Specifications (continued)

Rise/Fall Times

Time (nsec)	Symbol	Min	Max	Loading
ABn rise/fall	Tarf	6	---	C = 150 pF
DBn rise/fall	Tdrf	25	---	C = 150 pF
PCLK0 rise/fall	Tprf	---	30	C = 25 pF
TCLK rise/fall	Tprf	---	30	C = 25 pF
BLANK rise/fall	Tprf	30	---	C = 25 pF
LUMn rise/fall	Tprf	30	---	C = 25 pF
SYNC rise/fall	Tprf	30	---	C = 25 pF
RDY rise/fall	Tprf	30	---	C = 25 pF
HALT- rise/fall	Tprf	30	---	C = 25 pF
COL rise/fall	Tprf	30	---	C = 25 pF

Note:

Rise/fall times for maximums are between 0.4 and 2.4V.
Rise/fall times for minimums are between 10% and 90 % of final values.

Color Delay (phase-shifter)

Delay-line tuning range Ta = 0 to 70 C	210 ns phase difference between tap 1 and tap 15 for a settable DEL value between 0.0V to 6.0V
Phase-shift stability, 25 C to 55 C (DEL voltage initialized at 40 C for 336 deg. (14/15) of 4.43 Mhz (210 ns) between taps 1 and 15.)	205-220 ns phase difference between tap 1 and tap 15
Output Duty Cycle (COL, pin 43), COLCLK input (pin 3) = 50/50 4.433618 Mhz (± 1%) square wave	30/70 to 70/30 per cent. (high/low)